WHAT IS CLAIMED IS:

1. A ROM device having a repair function comprising:

a ROM cell array which has a plurality of memory cells;

a cell selecting section which selects at least one of the plurality of memory cells in response to an input address;

a sense amplifier section which senses data stored in the selected memory cell;

a repair control section which generates a first select signal in response to the input address; and

a first multiplexing section which selects and, in response to the first select signal, outputs one selected from the group consisting of an output of the sense amplifier section and a fixed voltage.

2. The ROM device according to claim 1, wherein the repair control section generates the first select signal having either one of two complementary states according to whether the input address corresponds to a defective cell, and wherein the first multiplexing section selects the fixed voltage when the first select signal is at a first logic state, and selects the output of the sense amplifier section when the first select signal is at a second logic state.

3. The ROM device according to claim 1, wherein the fixed voltage is one selected from ground voltage and an operating voltage of the device that is not ground, and wherein the fixed voltage is ground when a defective cell has a data "0"

defect, and the fixed voltage is the operating voltage when the defective cell has a data "1" defect.

4. The ROM device according to claim 1, wherein the cell selecting section includes:

a row decoder section which decodes a row address of the input address to select a row;

a row driving section which drives the selected row; and

a column decoder section which decodes a column address of the input address to select a column.

5. The ROM device according to claim 1, wherein the fixed voltage is one selected from ground and an operating voltage of the device that is not ground,

wherein the repair control section further includes a second multiplexing section for selecting either the ground or the operating voltage, and for transferring a selected signal to the first multiplexing section, and

wherein the repair control section generates a second select signal for controlling an output of the second multiplexing section.

6. The ROM device according to claim 5, wherein the repair control section generates the first select signal having either one of complementary states according to whether the input address corresponds to a defective cell,

wherein the first multiplexing section selects the fixed voltage when the first select signal is at a first logic state, and selects the output of the sense amplifier section when the first select signal is at a second logic state, and

wherein when the first select signal is at the first logic state, the second multiplexing section selects the operating voltage in response to the second select signal having the first logic state, and selects the ground voltage in response to the second select signal having the second logic state.

7. The ROM device according to claim 1, wherein the repair control section includes:

a plurality of fuse boxes corresponding to a number of bits in the input address, wherein each fuse box has two fuses;

a decoding block which has a plurality of NAND gates and receives outputs of the plurality of fuse boxes; and

a NOR gate which is connected to outputs of the NAND gates,

wherein when the input address designates a defective cell, either one of the two fuses in the respective fuse boxes corresponding to an input address bit is cut so as to output a signal of a first state, and

wherein when the input address designates a normal cell, the two fuses in the respective fuse boxes are not cut so as to output a signal of a second state.

8. The ROM device according to claim 5, wherein the repair control section includes:

a plurality of fuse boxes corresponding to a number of bits in the input address, wherein each fuse box includes first and second fuses;

a decoding block which has a plurality of NAND gates and receives outputs of the plurality of fuse boxes;

a NOR gate which is connected to outputs of the NAND gates to output the first select signal;

an NMOS transistor which has a gate connected to receive an output of the NOR gate and a source grounded;

a third fuse which has a first end connected to a drain of the NMOS transistor; and

a resistor which has a first end connected to a second end of the third fuse, and a second end connected to receive the operating voltage, the second select signal being outputted from an interconnection of the third fuse and resistor,

wherein when the input address designates a defective cell, either one of the first and second fuses in respective fuse boxes corresponding to an input address bit is cut so as to output a signal having a first state,

wherein when the input address designates a normal cell, the first and second fuses in the respective fuse boxes are not cut so as to output a signal of a second state,

wherein when a defective cell has a data "1" defect, the third fuse is cut so that the second select signal has a first logic state and the second multiplexing section selects the operating voltage, and

wherein when a defective cell has a data "0" defect, the third fuse is not cut so that the second select signal has a second logic state and the second multiplexing section selects the ground voltage.

9. A ROM device having a repair function comprising:

a cell array section which has a plurality of memory cells each storing a fixed data value;

a cell selecting section which selects at least one of the memory cells in response to an input address;

a sense amplifier section which senses data stored in the selected memory cell;

a repair control section which generates a first select signal and a second select signal in response to the input address; and

first and second multiplexing sections which operate responsive to the first and second select signals respectively,

wherein in response to the first select signal, the first multiplexing section selects and outputs one selected from the group consisting of an output of the sense amplifier section, and an output of the second multiplexing section, and

wherein in response to the second select signal the second multiplexing section selects one selected from the group consisting of a ground voltage and an operating voltage that is not ground.

10. The ROM device according to claim 9, wherein the repair control section generates the first select signal having a first logic state when the input address

corresponds to a defective cell and a second logic state when the input address corresponds to a normal cell, and wherein the repair control section generates the second select signal having either one of two complementary states according to a defect type of the defective cell when the first select signal has the first logic state.

11. The ROM device according to claim 10, wherein when the input address corresponds to a defective cell, the first select signal has the first logic state and the first multiplexing section selects the output of the second multiplexing section,

wherein when the defective cell has a data "1" defect, the second select signal has the first logic state and the second multiplexing section selects the operating voltage; and

wherein when the defective cell has a data "0" defect, the second select signal has the second logic state and the second multiplexing section selects the ground voltage.

12. The ROM device according to claim 9, wherein the ground voltage is a ground voltage of the device, and the operating voltage is formed in the device.

13. The ROM device according to claim 9, wherein the repair control section includes:

a plurality of fuse boxes which correspond to a number of bits in the input address;

a decoding block which has a plurality of NAND gates and receives outputs of the plurality of fuse boxes;

a NOR gate which is connected to outputs of the NAND gates to output the first select signal;

a first NMOS transistor which has a gate connected to receive an output of the NOR gate and a source grounded;

a select fuse which has a first end connected to a drain of the NMOS transistor; and

a resistor which has one end connected to a second other end of the select fuse, and a second end connected to receive the supply voltage, the second select signal being outputted from an interconnection of the select fuse and resistor, and

wherein each of the fuse boxes comprises:

a first CMOS transmission gate which receives an address bit;

a first address fuse which is connected to the first CMOS transmission gate;

a second CMOS transmission gate which an inverted version of the address bit;

a second address fuse which is connected to the second CMOS transmission gate; and

a second NMOS transistor which is connected between an interconnection node of the first and second address fuses and a ground voltage.

14. The ROM device according to claim 13, wherein when the input address corresponds to a defective cell, the first select signal has a first logic state and the first multiplexing section selects the output of the second multiplexing section,

wherein when the defective cell has a data "1" defect, the second select signal has the first logic state and the second multiplexing section selects the operating voltage; and

wherein when the defective cell has a data "0" defect, the second select signal has a second logic state and the second multiplexing section selects the ground voltage.

15. A repair method of a ROM device which includes a plurality of memory cells each storing a fixed data value, comprising:

generating a select signal according to whether a memory cell designated by an input address is a defective cell or a normal cell; and

selecting and outputting either a fixed voltage or a data value of the designated memory cell in response to the select signal.

16. The repair method according to claim 15, wherein the fixed voltage is a ground voltage when the defective cell is a data "0" defect, and wherein the fixed voltage is an operating voltage that is not ground when the defective cell is a data "1" defect.

17. The repair method according to claim 15, wherein when the designated memory cell is the data value, the select signal is inactivated and the data value is selected, and wherein when the designated memory cell is the defective cell, the select signal is activated and the fixed voltage is selected.

18. The repair method according to claim 17, further comprising generating a second select signal for selecting either one of a ground voltage or an operating voltage that is not ground according to a defect type of the defective cell.